In the claims:

Claims 1 to 20 (canceled).

21. (currently amended) A process of providing a high density module produced by a process comprising the steps of:

providing a circuit board having a substantially planar top surface for connection to at least one integrated circuit package;

providing an integrated circuit package having a pair of opposing major surfaces and at least one edge surface disposed between said opposing major surfaces, one of said at least one edge surface having at least one electrical terminal disposed thereon; and

electrically connecting said at least one electrical terminal on said at least one edge surface of said integrated circuit package to said top surface of said printed circuit board at an acute angle with said top surface of said printed circuit board..

22. (currently amended) The process as recited in claim 21 further including the step of electrically ~~and perpendicularly~~ connecting at least two said integrated circuit packages to said circuit board at a said edge.

23. (previously presented) The process as recited in claim 21 further including the step of disposing a solder ball between said side surface terminal of said integrated circuit package and said top of said circuit board.

24. (previously presented) The process as recited in claim 21 further including the step of disposing solder columns between said integrated circuit and said top of said circuit board.

25. (previously presented) The process as recited in claim 21 further including the step of integrally attaching at least three tabs to said circuit board.

26. (canceled)

27. (currently amended) The process as recited in claim 21 wherein said integrated circuit package is further defined as being connected at an acute angle between 30 and less than 90 degrees to said circuit board.

28 (previously presented) The process as recited in claim 21 wherein said at least one edge surface is four edge surfaces, each of said four edge surfaces disposed between said major surfaces to form a closed package with said major surfaces.

29. (new) A microelectronic package comprising:

a first microelectronic substrate;

a second microelectronic substrate that is oriented at an acute angle relative to the first microelectronic substrate; and

a plurality of solder bumps between the first and second microelectronic substrates, adjacent an edge of the second microelectronic substrate, that directly connect the second microelectronic substrate to the first microelectronic substrate and that are confined to within the edge of the second microelectronic substrate.

30. (new) A microelectronic package according to claim 29 wherein the acute angle includes a vertex and wherein the edge of the second microelectronic substrate is adjacent the vertex.

31. (new) A microelectronic package according to claim 29 wherein the plurality of solder bumps is a plurality of first solder, the microelectronic package further comprising:

a third microelectronic substrate on the first microelectronic substrate that laterally overlaps the second microelectronic substrate; and

a plurality of solder bumps that directly connect the third microelectronic substrate to the first microelectronic substrate.

32. (new) A microelectronic package according to claim 31 wherein the second and third microelectronic substrates are oriented parallel to one another at the acute angle relative to the first microelectronic substrate.

33. (new) A microelectronic package according to claim 32 wherein the plurality of second solder bumps are between the first and third microelectronic substrates, adjacent an edge of the third microelectronic substrate and are confined to within the edge of the third microelectronic substrate.

34. (new) A microelectronic package according to claim 33 wherein the acute angle includes a vertex and wherein the edge of the third microelectronic substrate is adjacent the vertex.

35. (new) A microelectronic package according to claim 31 wherein the third microelectronic substrate extends between the first and second microelectronic substrates.

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36. (new) A microelectronic packaging method comprising:

orienting a second microelectronic substrate at an acute angle relative to a first microelectronic substrate such that a plurality of solder bumps extend between the first and second microelectronic substrates, adjacent an edge of the second microelectronic substrate; and

reflowing the plurality of solder bumps to connect the second microelectronic substrate to the first microelectronic substrate while confining the plurality of solder bumps to with the edge of the second microelectronic substrate during reflowing.